

REMARKS

In response to the prior art rejections, no claims have been amended. Claims 1-30 remain in this application. Applicant respectfully requests that the above-identified application be considered in view of the following remarks.

The 35 U.S.C. §102(b) Rejections

Claims 1-30 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,210,829 to Bitner ("Bitner"). Bitner discloses a tape drive with an electronic buffer that temporarily stores data transferred between the host computer and the tape driver's magnetic tape. During a write transaction, in which the host computer sends data to the tape for storage, the buffer receives that data sent over the system bus by the host computer, and it temporarily stores the data until the tape mechanism has ramped up to its write velocity. The buffer having an adjustable threshold otherwise known as a "watermark" which determines the level of data that must be present in the buffer before the mechanical assembly of the tape drive will begin to ramp the tape up to its write velocity. When the write velocity is achieved, the data in the buffer is transferred onto the tape, and the buffer is emptied so that it may receive additional data.

These rejections are traversed, in part, because the cited reference fails to teach or suggest features of the present invention for loading a memory buffer as recited in the claims. For example, the cited reference fails to teach or suggest a memory buffer that has a watermark with a first watermark value and can receive an advance indication of a memory service interruption. Moreover, the cited reference fails to teach or suggest that based at least in part on the received advance indication of the memory service interruption, the watermark can be modified to have

a second watermark value different from the first watermark value.

In rejecting independent claim 1 and claims 2-10, which ultimately depend from independent claim 1, the Office Action states that Bitner teaches a method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value (Examiner cites to fig. 1 element 34 and fig. 2 and col. 8 lines 10-20), the method comprising: receiving an advance indication of a memory service interruption (Examiner cites to fig. 5 elements 74, 76); and based at least in part on the received advance indication of the memory service interruption, modifying the watermark to have a second watermark value different from the first watermark value (Examiner cites to fig. 5 elements 74, 76 and fig. 3 and col. 10 lines 30-43).

Applicant respectfully disagrees. Bitner does not teach a method where the watermark is changed based on a received advance indication of a memory service interruption. In Bitner, the watermark is changed based on whether overflow has been detected. There is nothing "advance" about an "overflow" condition. If the "overflow" condition is considered to be a "memory service interruption," then the modification of the watermark occurs after such an interruption occurs and not in advance of it as recited in the claims.

In rejecting independent claim 11 and claims 12-14, which ultimately depend from independent claim 11, the Office Action states that Bitner teaches a method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value (Examiner cites to fig. 1 element 34 and fig. 2 and col. 8 lines 10-20), the method comprising: modifying the watermark to have a second watermark value prior to the occurrence of a memory service interruption, the second watermark value being different than the first watermark value (Examiner cites to fig. 5 elements 74, 76 and fig. 3 and col. 10 lines 30-43); and modifying the

watermark to have a third watermark value subsequent to the occurrence of the memory service interruption, the third watermark value being different than the second watermark value (Examiner cites to fig. 4 and col. 21 lines 29-31 and fig. 5 elements 74, 80 and col. 21 lines 16-31). Applicant respectfully disagrees. Similarly to independent claim 1, the watermark is modified to a second watermark value prior to the occurrence of a memory service interruption. In Bitner, the watermark value is modified (see blocks 76 and 80 in Fig. 5b) in response to an overflow condition (see block 74 in Fig. 5a). Thus, if the overflow condition is considered to be a memory service interruption, then clearly the modification of the watermark value occurs after the overflow condition and not prior to it as recited in the claims.

In rejecting independent claim 15 and claims 16-18, which ultimately depend from independent claim 15, the Office Action states that Bitner teaches an apparatus to control the loading of a memory buffer, comprising: a memory buffer (Examiner cites to fig. 1 element 34); and a memory controller, coupled to said memory buffer (Examiner cites to fig. 1 element 32), including a watermark register (Examiner cites to fig. 1 and col. 7 lines 53-58, stating “wherein buffer watermark is adjustable; such as 0 Kb buffer watermark or 430 Kb buffer watermark, therefore it is obviously the controller has a watermark register”); a first register, coupled to said watermark register, to store a first watermark value (Examiner cites to fig. 1 elements 34, 26 and fig. 2 and col. 8 lines 10-20, stating “wherein the first watermark value 0 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a first register”); and a second register, coupled to said watermark register, to store a second watermark value (Examiner cites to fig. 1 elements 34, 26 and fig. 3 and col. 10 lines 30-43, stating “wherein the second watermark 430 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a second register”). Applicant

respectfully disagrees. Bitner does not teach an apparatus comprised of a memory controller coupled to a memory buffer, but instead concerns a buffer between a system bus and a tape drive 42. (See Fig.1).

In rejecting independent claim 19 and claim 20, which ultimately depends from independent claim 19, the Office Action states that Bitner teaches a system to process video signals, the system comprising: a processor (Examiner cites to fig. 1 element 36); a memory, coupled to said processor (Examiner cites to fig. 1 element 22); a memory buffer, coupled to said memory (Examiner cites to fig. 1 element 34); and a memory controller, coupled to said memory buffer (Examiner cites to fig. 1 element 32), including a watermark register (Examiner cites to fig. 1 and col. 7 lines 53-58, stating "wherein buffer watermark is adjustable; such as 0 Kb buffer watermark or 430 Kb buffer watermark, therefore it is obviously the controller has a watermark register"); a first register, coupled to said watermark register, to store a first watermark value (Examiner cites to fig. 1 elements 34, 26 and fig. 2 and col. 8 lines 10-20, stating "wherein the first watermark value 0 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a first register"); and a second register, coupled to said watermark register, to store a second watermark value (Examiner cites to fig. 1 elements 34, 26 and fig. 3 and col. 10 lines 30-34, stating "wherein the second watermark 430 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a second register"). Applicant respectfully disagrees. By similar reasoning as claim 15 and claims 16-18, Bitner does not teach a system comprised of a memory controller coupled to a memory buffer, but instead concerns a buffer between a system bus and a tape drive 42. (See Fig. 1).

In rejecting independent claim 21 and claim 22, which ultimately depends from independent claim 21, the Office Action states that Bitner teaches a computer-

readable medium storing a plurality of instructions to be executed by a processor to control a memory buffer having a watermark with a first watermark value and a below-watermark burst size with a first burst value (Examiner cites to fig. 1 elements 36, 40, 34 and fig. 2 and col. 8 lines 10-20), said plurality of instructions comprising instructions to: receive an advance indication of a memory service interruption (Examiner cites to fig. 5 elements 74, 76); and based at least in part on the received advance indication of the memory service interruption, modify the watermark to have a second watermark value different from the first watermark value (Examiner cites to fig. 5 elements 74, 76 and fig. 3 and col. 10 lines 30-43). Applicant respectfully disagrees. By similar reasoning as in claim 1 and claims 2-10, Bitner does not teach a method where the watermark is changed based on a received advance indication of a memory service interruption. In Bitner, the watermark is changed based on whether overflow has been detected. There is nothing "advance" about an "overflow" condition in the Bitner reference. The watermark value is changed only after such a condition occurs.

In rejecting independent claim 23 and claims 24-27, which ultimately depend from independent claim 23, the Office Action states that Bitner teaches an apparatus comprising: a memory buffer (Examiner cites to fig. 1 element 34); and a memory controller coupled to said memory buffer, said memory controller to operate in a first mode maintaining a first level of buffering in said memory buffer and to switch to a second mode maintaining a second level of buffer that is higher than the first level of buffering in response to an advance indication of a memory service interruption (Examiner cites to fig. 1 element 32 and fig. 5 elements 74, 76 and fig. 3 and column 10 lines 30-43). Applicant respectfully disagrees. By similar reasoning as to claims above, Bitner does not teach a system comprised of a memory controller coupled to

a memory buffer, and does not teach the modification of a buffering level in advance of a memory service interruption as recited in these claims.

In rejecting independent claim 28 and claims 29-30, which ultimately depend from independent claim 28, the Office Action states that Bitner teaches an apparatus comprising: a video stream buffer (Examiner cites to fig. 1 elements 34, 26 and col. 25 lines 14-19, stating "wherein the buffer 34 can be a video stream buffer because the tape drive 26 also be implemented in other electromechanical devices") a memory controller to occasionally perform an operation causing a memory services interruption (Examiner cites to fig. 5 elements 74, 76); and control logic coupled to said video stream buffer to maintain a first level of buffering in a first mode and to maintain a higher level of buffering prior to said memory controller performing said operation causing said memory service interruption (Examiner cites to fig. 1 elements 32 and col. 6 lines 59-67). Applicant respectfully disagrees. By similar reasoning as claims 15—20 and claims 23-27; Bitner does not teach a system comprised of a memory controller coupled to a memory buffer, but instead concerns a buffer between a system bus and a tape drive 42. (See Fig. 1).

The Office Action rejected the remaining claims on analogous grounds. Because all remaining claims ultimately depend upon the independent claims, Applicant respectfully requests that the rejection of these claims be reconsidered. Accordingly, reconsideration and withdrawal of the rejection of claims 2-10, 12-14, 16-18, 20, 22, 24-27, 29, and 30 which ultimately depend from claims 1, 11, 15, 19, 21, 23, and 28, respectively under 35 U.S. C. § 102(b) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this

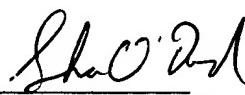
application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.1.7 to Deposit Account No. 11-0600.

Respectfully submitted,

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